LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. - 10 Canceled.

11. (Currently Amended) A process for manufacturing a planar power semiconductor device comprising:

providing a semiconductor die including an epitaxially grown silicon layer of a first conductivity formed over a ~~silicon~~ substrate;

designating an active area, said active area being a portion of said epitaxially grown silicon layer in which channel regions are formed;

implanting dopants of a second conductivity in all of said active area of said epitaxially grown silicon layer;

forming a plurality of spaced channel regions of said second conductivity in said active area of said epitaxially grown silicon layer, each channel region being spaced from another channel region by a first conductivity region in said epitaxially grown silicon layer;

forming a source region of said first conductivity in each of said channel regions, each source region being less wide and less deep than a channel region in which it is formed; and

forming a horizontally oriented gate structure over said epitaxially grown silicon layer and at least each channel region.

12. (Previously Presented) A process according to claim 11, further comprising forming a field oxide termination structure at the edge of said active area prior to said implanting step.

13. (Previously Presented) A process according to claim 11, further comprising forming a field oxide termination structure at the edge of said active area after said implanting step.

14. (Previously Presented A process according to claim 11, wherein said gate structure comprises a gate oxide, said gate oxide being formed after said implanting step.

15. (Previously Presented) A process according to claim 12, wherein said field oxide is formed over said epitaxially grown silicon and etched to provide a window over said active area, wherein said dopants of said second conductivity are implanted through said window.

16. (Previously Presented) A process according to claim 11, wherein said dopants of said second conductivity are comprised of boron.

17. (Previously Presented) A process according to claim 11, wherein said dopants of said second conductivity type are comprised of either arsenic or phosphorous.

18. (Currently Amended) A process according to claim 11, further comprising, forming an oxide interlayer over said ~~active area~~ gate structure; opening windows in said oxide interlayer over at least said source regions; and forming a source contact over said ~~active area~~ ~~region~~ oxide interlayer and a heavy base region.